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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,209	03/07/2001	Thomas Peter Haneder	GR 98 P 2499 P	4018

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EXAMINER
LE, THAO X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/801,209	Applicant(s) HANEDER ET AL.
	Examiner Thao X Le	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,9 and 10-11* is/are rejected.

7)☒ Claim(s) *2,7 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I claims 1-12 in Paper No. 9 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

2. Claim 8 is objected to because of the following informalities: 'layerand' should be 'layer and'. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims1, 6,10, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6011285 to Hsu et al.

Regarding to claim 1, Hsu discloses a ferroelectric transistor in fig. 12, comprising: a semiconductor substrate 80 having a surface and having two source/drain (S/D) regions 42/46

therein, a first gate intermediate layer 50/52 and a first gate electrode 54 configured on surface of semiconductor substrate between source/drain regions, and first gate intermediate layer including at least one ferroelectric layer 52, a second gate intermediate layer 124 and a second gate electrode 48 configured between S/D regions and extending in a direction of a line running between S/D regions, first gate intermediate layer also extending in the direction of line running between S/D regions, second gate intermediate layer including a dielectric layer, and first gate electrode 54 connected to second gate electrode.

Regarding to claims 6 and 10, Hsu disclose inherently the ferroelectric transistor comprising a diode structure consisting of first gate electrode 54 and second gate electrode 48.

Regarding to claim 11, Hsu discloses a memory cell configuration including a plurality of memory cells, each one of plurality of memory cells including a ferroelectric transistor as discussed in claim 1.

5. Claims 1, 3 and 8 rejected under 35 U.S.C. 102(b) as being anticipated by EPO Pub. No. 0540993 to Argos.

Regarding to claim 1, Argus discloses a ferroelectric transistor in fig. 9, comprising: a semiconductor substrate 10 having a surface and having two source/drain (S/D) regions 60/70 therein, a first gate intermediate layer 20/30 and a first gate electrode 50 configured on surface of semiconductor substrate between source/drain regions, and first gate intermediate layer including at least one ferroelectric layer 30, a second gate intermediate layer 80 and a second gate electrode 100 configured between S/D regions and extending in a direction of a line running between S/D regions, first gate intermediate layer also extending in the direction of line running

between S/D regions, second gate intermediate layer including a dielectric layer, and first gate electrode 50 connected to second gate electrode 100.

Regarding to claim 3, Argus discloses a ferroelectric transistor in fig. 9 wherein first gate intermediate layer includes a dielectric layer 20 configured between surface of semiconductor substrate 10 and ferroelectric layer 30.

Regarding to claim 8, Argus discloses a ferroelectric transistor in fig. 9 comprising an auxiliary layer 40 disposed between ferroelectric layer and first gate electrode.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4-5, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US6011285 to Hsu et al. in view of EPO Pub 0540993 A3 to Argos.

Regarding to claims 4-5 and 9, Hsu disclose the dielectric layer 124 consisting of silicon dioxide, fig. 12, of second gate intermediate layer is formed as a continuous layer.

However, Hsu does not expressly disclose the ferroelectric transistor wherein first gate intermediate layer includes a dielectric layer configured between surface of semiconductor substrate and ferroelectric layer consisting of PZT, SBT.

But Argus reference discloses in fig. 9 a ferroelectric transistor wherein the first gate intermediate layer 20/30 includes a dielectric layer 20 selected from the group

consisting of CeO_2, ZrO_2, Y_2O_3, and $SrTiO_3$, claim 2, configured between surface of semiconductor substrate and ferroelectric layer consisting of PZT, claim 3. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the dielectric 20 teaching of Argus in the first gate intermediate layer of Hsu, because it would have prevented the inter-diffusion between the ferroelectric material and the silicon substrate as taught by Argus, column 2 line 22.

Allowable Subject Matter

8. Claims 2, 7 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- Claims 2, the prior arts fail to disclose second gate intermediate layer includes two substructures configured mirror-symmetrically in the relation to first gate intermediate layer.
- Claims 7, the prior art fail to disclose the first gate electrode includes polycrystalline silicon including doping of a first conductivity and second gate electrode includes polycrystalline silicon including doping of a second conductivity
- Claims 12, the prior arts fail to disclose the memory cells including a selection transistor connected between second gate electrode of ferroelectric transistor.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. US 5973379

b. US 5365094

c. US 5973379

d. US 6278164

e. US 6074885

f. US 5449935

g. US 5932904

h. US 5989927

i. US 5900656

j. US 5541870

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
September 19, 2002

PHAT X. CAO
PRIMARY EXAMINER